



Lab-03

Particular Logic Gates

Chia-Chun Tsai

Objectives



- Understand particular logic gates, **Buffer**, **Tristate-Buffer**, **Tristate-NOT**, **Schmitt-trigger NOT**, and **Schmitt-trigger NAND** and their **truth tables**.
- Understand **Buffer with open collector** and its **truth tables**.
- Measure **the transfer voltage of a logic**, **V_f** .
- Understand **a signal whether is passed or not** by controlling the gate.

Chia-Chun Tsai

2

What are for Particular Gates



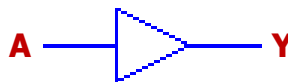
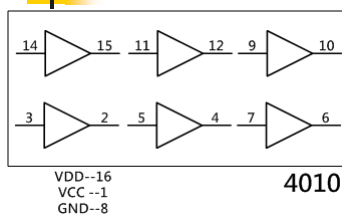
- Besides those **Basic Logic Gates** NOT, AND, OR, NAND, NOR, and XOR, the **Particular gates** are:

**Buffer, Tristate Buffer, Tristate NOT
Schmitt-Trigger NOT, and
Schmitt-Trigger NAND.**

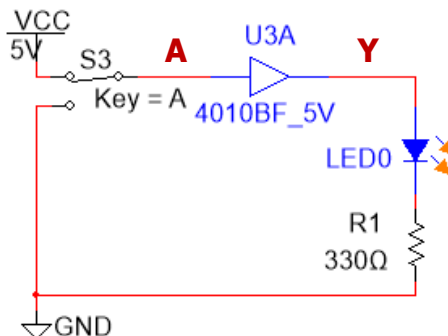
Chia-Chun Tsai

3

Buffer CMOS IC-4010



A	Y=A
0	0
1	1



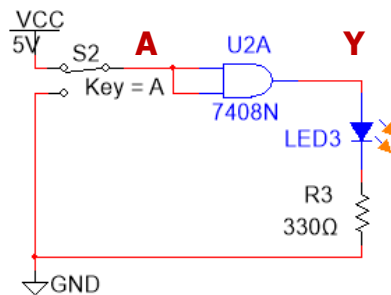
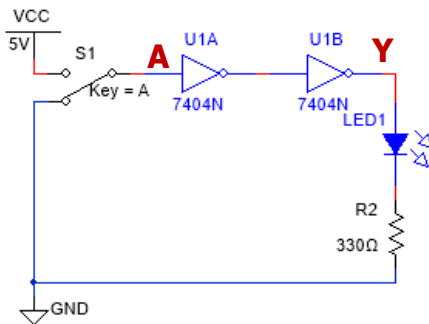
Chia-Chun Tsai

4

Equivalent Buffer



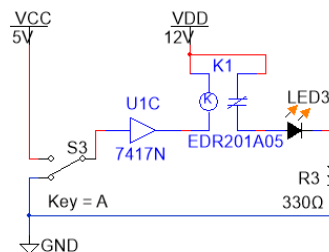
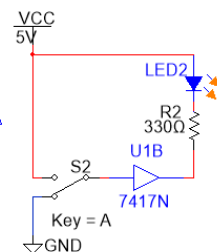
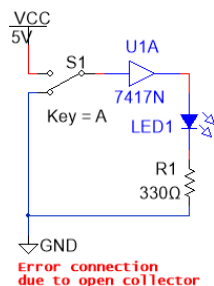
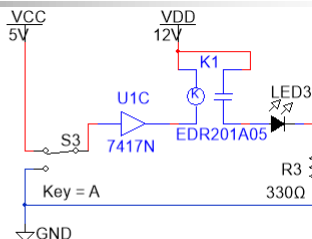
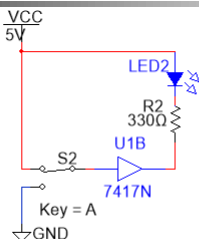
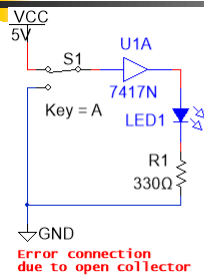
A	Y=A
0	0
1	1



Chia-Chun Tsai

5

Buffer with Open Collector

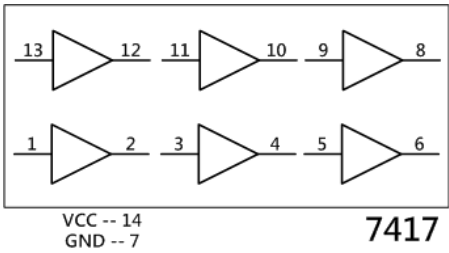


Chia-Chun Tsai

6

Buffer with Open Collector





A	Y=A
0	0
1	1

A	Y=A
0V	0.15V
5V	4.41V

7417 needs power supply

VCC pin-14 +5V

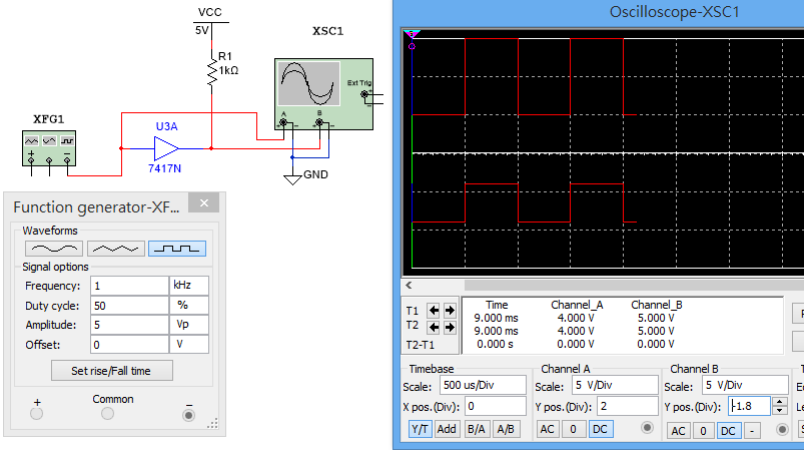
GND pin-7 0V

Output connects a loading (e.g. 1kohm) to +5V

Buffer with open collector

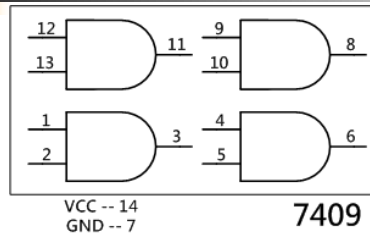


A	Y=A
0V	0.15V
5V	4.41V



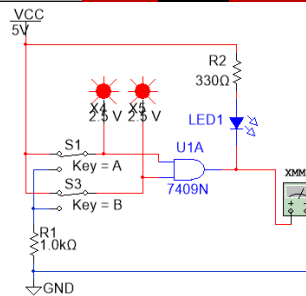


AND with Open Collector



A	B	Y=AB
0	0	0
0	1	0
1	0	0
1	1	1

Output connects a 1kohm to +5V

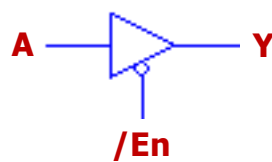


Chia-Chun Tsai

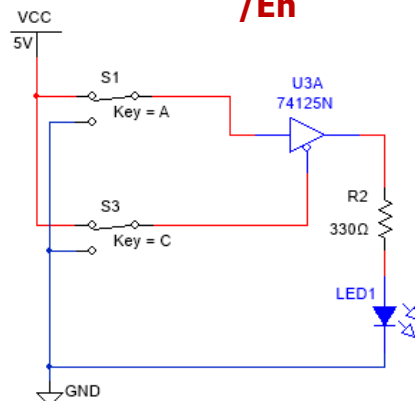
A	B	Y=AB
0V	0V	0.15V
0V	5V	0.15V
5V	0V	0.15V
5V	5V	4.55V

9

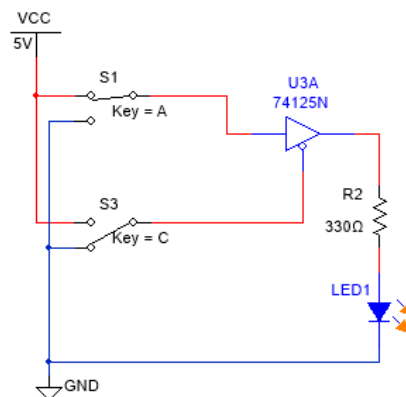
Tristate Buffer



/En	A	Y=A
0	0	0
0	1	1
1	0	X (open)
1	1	X (open)



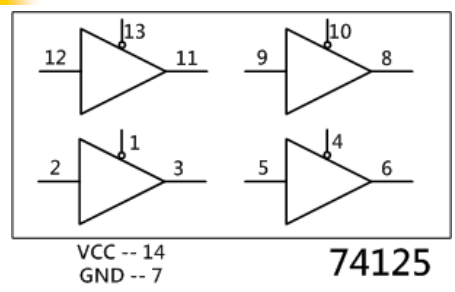
Chia-Chun Tsai



10



Tristate Buffer



/En	A	Y=A
0	0	0
0	1	1
1	0	X (open)
1	1	X (open)

/En	A	Y
0V	0	0.15V
0V	1	4.41V
0V		
5V	0	X (open)
5V	1	X (open)
5V		X (open)

The IC needs power supply

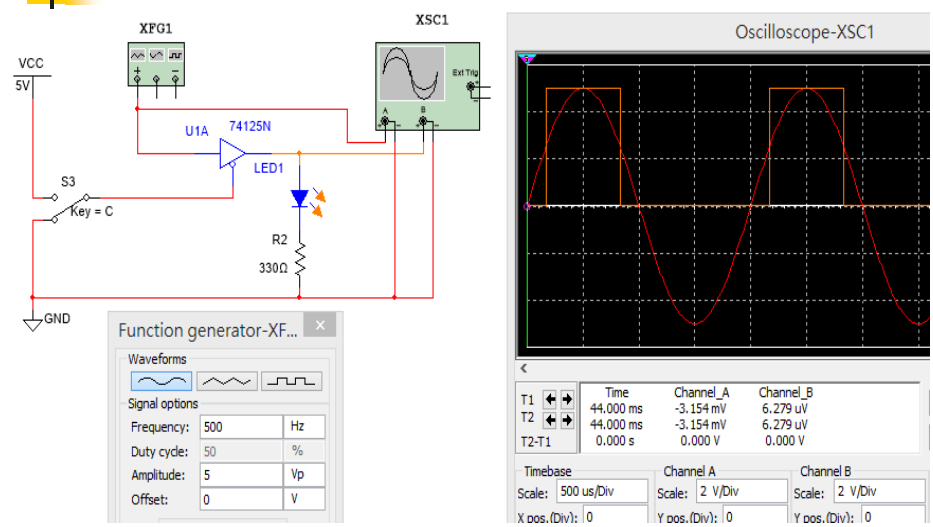
VCC pin-14 +5V

GND pin-7 0V

Chia-Chun Tsai



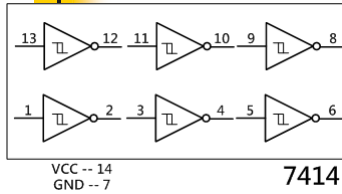
Signal Pass by Tristate Buffer



Chia-Chun Tsai

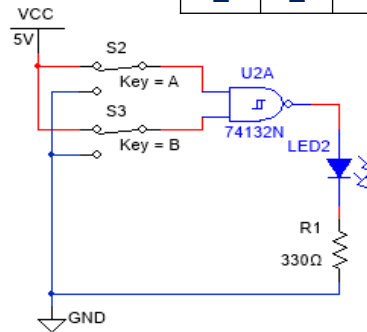
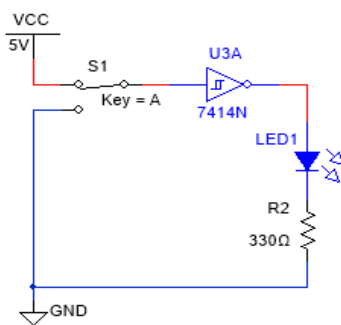


Schmitt-Trigger Gates



A	Y = /A
0	1
1	0

A	B	Y = /(AB)
0	0	1
0	1	1
1	0	1
1	1	0

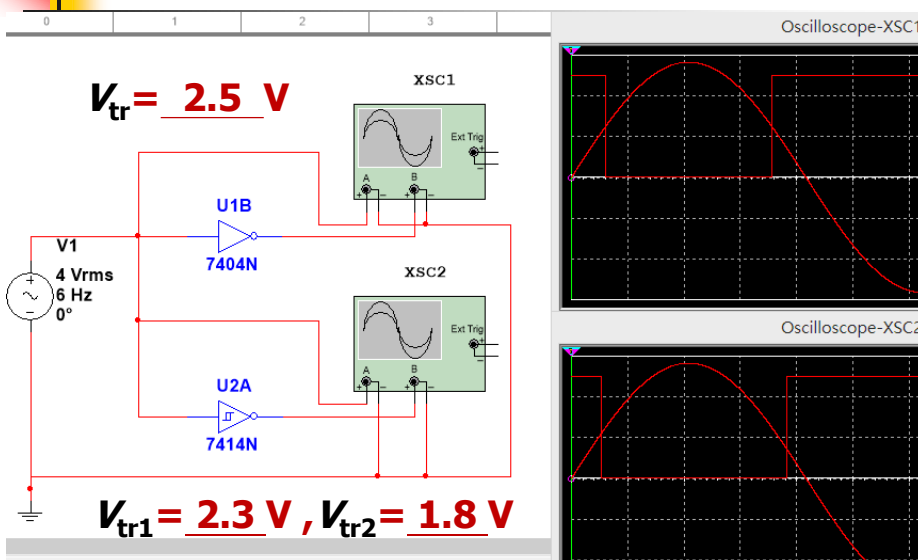


Chia-Chun Tsai

13



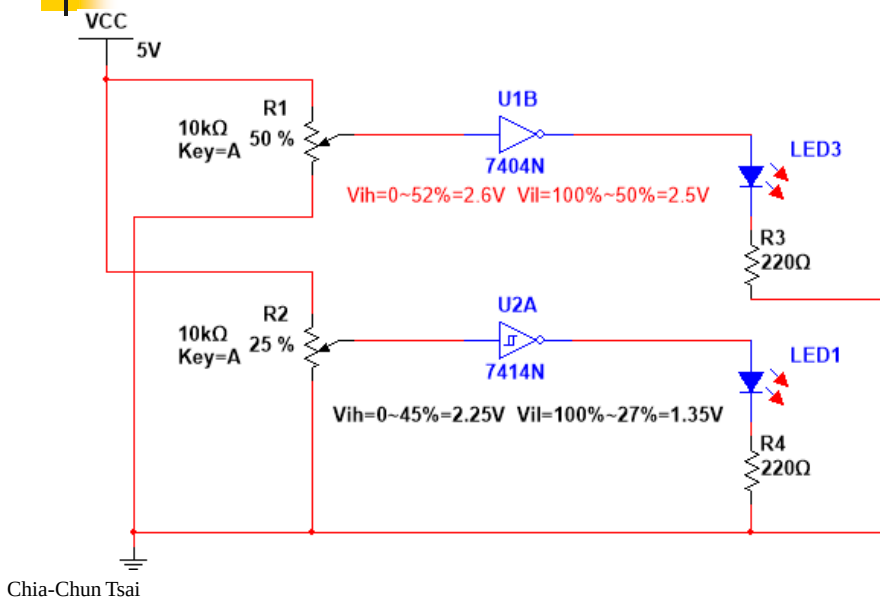
Different Transfer Voltages



Chia-Chun Tsai

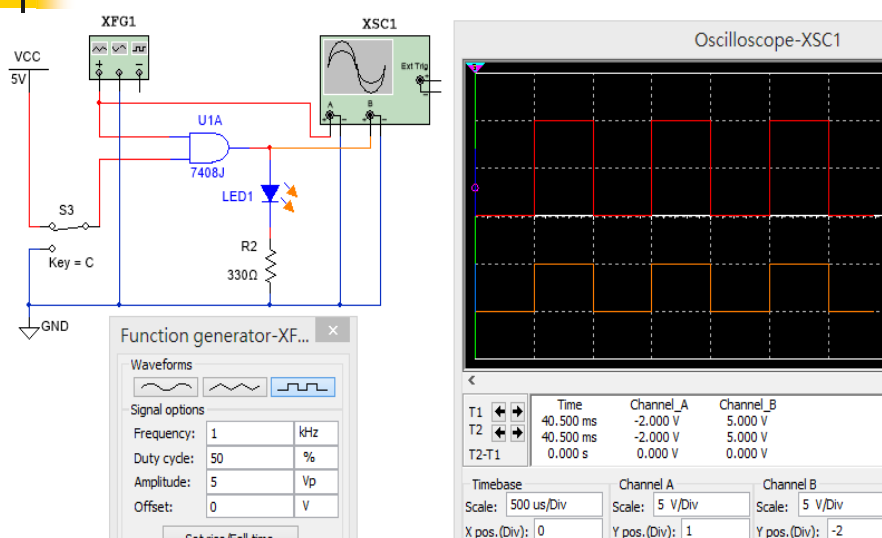
14

Different Transfer Voltages



15

Signal Pass by AND Gate

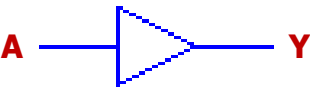


Chia-Chun Tsai

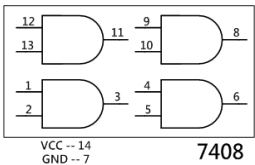
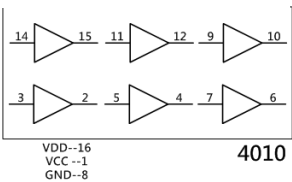
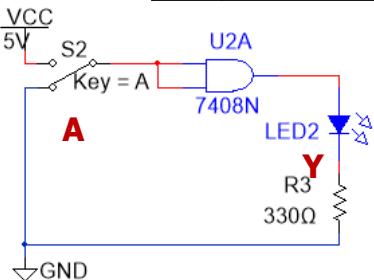
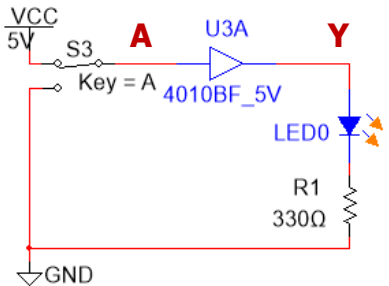
16



Experiment-1 Buffer



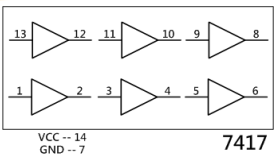
A	LED ON/OFF
0V	
5V	



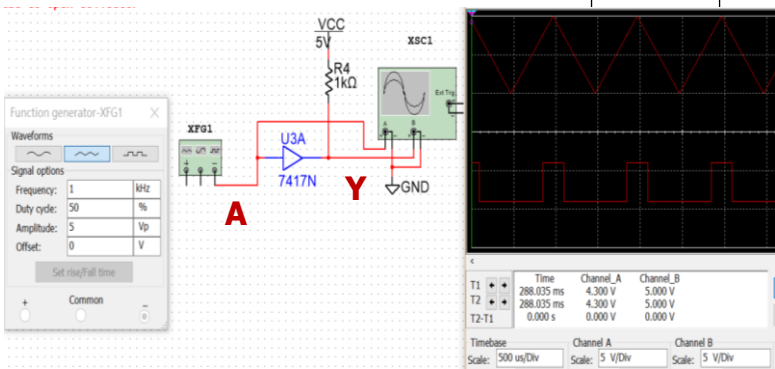
Chia-Chun Tsai

17

Experiment-2 Buffer with Open Collector



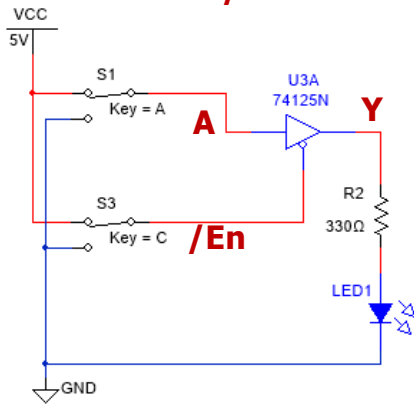
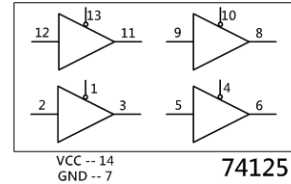
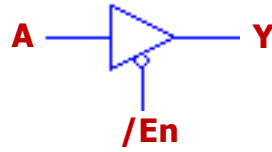
A	Y (Scope)
0V	
5V	
waves	



Chia-Chun Tsai

18

Experiment-3 Tristate Buffer



Chia-Chun Tsai

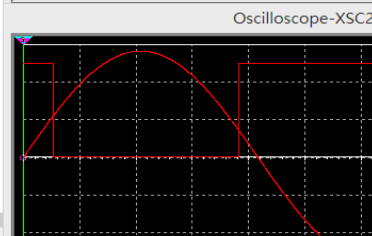
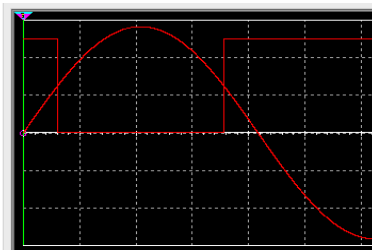
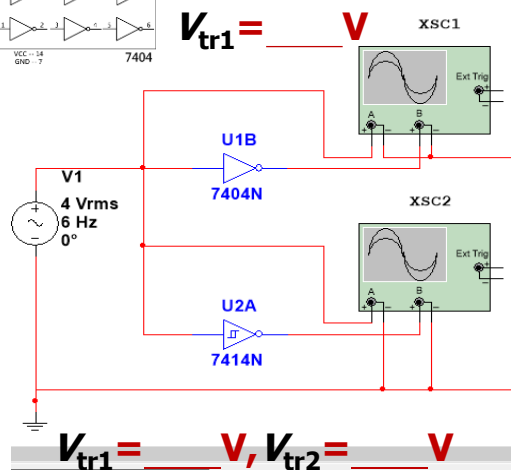
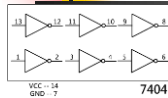
Wave: Square 10Hz/5V

/En	A	Y (LED1)
0V	0V	
0V	5V	
0V	wave	
5V	0	
5V	1	
5V	wave	

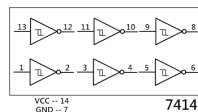
19

Experiment-4

Different Transfer Voltages



Chia-Chun Tsai



20